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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/714,615 | 11/18/2003 | Nam Sik Kim | 1261.0007-01 | 3669 |

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
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WASHINGTON, DC 20005

| EXAMINER | |
|---|---|
| DOLAN, JENNIFER M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/714,615 | KIM, NAM SIK | |
| | Examiner | Art Unit | |
| | Jennifer M. Dolan | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 2* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/155,016.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,872,044 to Hemmenway et al. (cited by applicant) in view of U.S. Patent No. 6,060,749 to Wu.

Hemmenway discloses a SOI wafer having a first silicon layer (11), a buried insulating film (12), and a second silicon layer (2 and 14); a trench in the second silicon layer (figures 6 and 7); a first silicide layer comprising titanium formed on the sidewalls of the trench (column 5, lines 20-35); a device isolation film formed by filling the trench (column 1, lines 30-55; column 6, lines 8-25) and defining an active region of the wafer (figure 9; transistor region between trenches); a gate electrode (31) having a gate insulation film (4) formed on the active region (figure 4); an insulation spacer (51) formed at the sidewalls of the gate electrode (figures 7-9); and impurity junction regions (42, 43) formed at both sides of the gate electrode and the impurity region (figures 5-9).

Hemmenway fails to disclose a second silicide layer formed on the gate electrode and impurity regions.

Wu teaches an SOI transistor having silicide layers (34, 36) comprising Ti, Co, W, or Ni (column 5, lines 10-20) formed on the gate electrode and impurity regions (figure 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hemmenway such that silicide layers are formed on the gate, source, and drain regions, as taught by Wu. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide silicide layers on the gate, source, and drain regions in order to reduce the parasitic resistance involved with contacting the gate, source, and drain, such that high performance devices are possible (see Wu, column 3, lines 8-22).

3. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,017,801 to Youn (cited by applicant) in view of Wu.

Youn discloses a MOSFET/semiconductor device comprising a trench (at 22) formed by removing a portion of the silicon substrate (figure 3B); a first silicide layer (vertical portion of 28a) formed on the sidewalls of the trench (figure 3B); an isolation film formed from filling the trench (STI 22), defining an active region (transistor region between STIs, figures 5C, 5D); a gate electrode (24) having a gate insulation film (23); an insulating spacer at the sidewalls of the gate electrode (26); impurity junction regions (25, 27a) formed at both sides of the gate electrode (figures 4B, 4C); and a second silicide layer (28a; horizontal regions) formed on the gate, source, and drain regions (figure 5D), wherein the silicide comprises Ti, Co, or Ni (column 4, lines 28-35).

Youn fails to disclose that the device is formed on an SOI substrate.

Wu discloses a MOSFET provided on an SOI substrate (see column 1, lines 10-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the MOSFET of Youn such that it is provided in a SOI substrate, as

suggested by Wu. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a SOI substrate, because Wu teaches that MOSFETs are advantageously fabricated with SOI substrates in order to alleviate short channel effects and reduce power consumption (see Wu, column 1, lines 29-54). Since the MOSFET structure of both Youn and Wu are substantially similar, it is well within the purview of a person skilled in the art to use an SOI substrate with the structure of Youn.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 4,839,309 to Easter et al. discloses silicide layers formed as part of a trench isolation structure sidewall.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800